REMARKS

In the interest of clarity, the following Item Numbers correspond to the Examiner's Item Numbers in the November 17, 2004 non-final Office Action:

1. The Examiner notes that the November 17, 2004 non-final Office Action is responsive to an Amendment filed 08/04/2004. Applicant notes that while Applicant did not file an Amendment on 08/04/2004, the Examiner's Advisory Action was dated the same. If necessary, Applicant thus seeks clarification.

2. Claims **1-20** are pending.

With this Response:

- Applicant withdrew Claim 9;
- Applicant amended Claims 10-12 to incorporate the limitations of Claim 8, as the Examiner suggested.
- Applicant made other, non-substantive amendments to each of the remaining claims to increase clarity.

3. The Examiner objected to the drawings under 37 CFR 1.83(a) for apparently not "show[ing] every feature of the invention specified in the claims." Respectfully, Applicant traverses and requests withdrawal.

More specifically, the Examiner failed to identify what element, if any, appears in Claim 9 but not in the figures. Accordingly, Applicant respectfully asks the Examiner to either identify the missing element, if any, or withdraw the objection. However, since the Examiner required "[c]orrected drawings sheets in compliance with 37 CFR 1.121(d)" in order "to avoid abandonment of the application" and stated "[t]he objection to the drawings will not be held in abeyance," Applicant respectfully withdrew Claim 9 in order to provide the Examiner a greater chance to now clarify or withdraw the objection.

4-5. The Examiner rejected Claims 1-2, 6-8, 13-15, and 17-19 under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 5,539,685 to Otaguro ("Otaguro"). Respectfully, Applicant traverses and requests withdrawal.

As a preliminary matter, Applicant notes that since the Examiner limited the Examiner's analysis to Otaguro's FIG. 10, Applicant will likewise limit Applicant's response thereto.

First, the Examiner repeatedly asserts that a first operand in LLT register 103 and a second operand in QR register 101 are in fixed-point formats. However, Otaguro does not

support this assertion. For example, Otaguro only identifies the first operand in QR register 101 as a "multiplier" (*see, e.g., Col. 9, line 14*) and the second operand in LLT register 103 as a "multiplicand" (*see, e.g., Col. 9, line 26*). Indeed, Otaguro does not specify a fixed-point format for either of these operands, and the Examiner is without support to assert otherwise.

Second, the Examiner asserts that Otaguro's adder 106 "perform[s] at least partially the arithmetic operation of the first and second operands (106 for summing or accumulating all the partial products terms)." However, Otaguro does not support this assertion. For example:

> TMPR is an accumulation register 105 for accumulating the output from an adder (ADDER) 106. The adder (ADDER) 106 adds the values output from the shifter (SHF) 104 to the values output from the accumulation TMPR-register 105 and stores the result in the accumulation TMPR-register 105.

Col. 9, lines 30-34. In other words, the TMPR register 105 i) accumulates "the output" from the adder 106 and ii) stores "the result" from adding the value output from the SHF register 104 to the values output from the adder 106. Identifying "the output" and "the result" would appear to refer to completed calculations. Indeed, Otaguro does not specify partial ALU calculations, and the Examiner is without support to assert otherwise

Third, the Examiner repeatedly asserts that Otaguro's "computation of 108 and 109 does not require any parameters from the multiplier {104, 105, and 106}; therefore it is independent and substantially in parallel." However, Otaguro does not support this assertion. For example:

> In order to detect an overflow during a multiplication operation, the multiplier device 100 of the present invention is equipped with an overflow detector (OVFD) 107 comprising a mask generator (MSIA) 108, an AND-operator 109...**and an OR-gate (OR) 110**...

Col. 9, lines 35-43 (emphasis added). In other words, even if computations in the MSKA register 108 and the AND gate 109 do not require parameters from registers 104 and 105 or the adder 106, as asserted by the Examiner, this is irrelevant. These are NOT the outputs from the overflow detector 107. Rather, they are intermediate calculations within the overflow detector 107. More specifically, Otaguro's overflow detector 107 comprises the afore-mentioned three elements—namely, i) the MSKA register 108, ii) an AND gate 109, and iii) an OR gate 110. Otaguro does not detect an overflow condition based on the MSKA register 108 and the AND gate 109 alone, but by performing an OR operation between the output of the AND gate 109 and **the carry output from the adder 106**. In fact, it would have been difficult for Otaguro to have been clear on this specific point:

> In this manner, the occurrence of an overflow during multiplication can be detected by the overflow detection function of the multiplier device 100 of this embodiment by performing an OR operation between the output of the operator AND and the carry output from the adder (ADDER) 106.

Col. 9, lines 54-59. This *serial processing* is also readily apparent in Otaguro's FIG. 10, in which the output from the overflow detector 107 can be readily seen at the output of the OR gate 110 (identified as "OVF" in FIG. 10 and repeatedly identified as "the output OVF" throughout Otaguro). This output OVF, however, necessarily requires the carry bit from the adder 106. Thus, Otaguro's ALU calculations from the adder 106 and overflow calculations from the overflow detector 107 are *serial process*, as Otaguro cannot complete the latter without first completing the former. Indeed, Otaguro does not specify parallel processing, and the Examiner is without support to assert otherwise.

In sum, Applicant respectfully believes the Examiner's rejection is in error because the Examiner failed to recognize that Otaguro fails to anticipate or render obvious at least the following:

1. **fixed-point formats;**
2. **partial ALU calculations, and**
3. **parallel processing.**

More specifically, ALU Operations and Overflow Detection are **dependent, serial** processes in Otaguro, much like in U.S. Pat. No. 5,907,498 to Rim, which the Examiner has now withdrawn. In contrast, each of Applicant's rejected independent claims contains **partial ALU calculations** and **parallel processing** language, which Applicant asserts is not anticipated or rendered obvious by Otaguro. For example, Applicant asks the Examiner to consider Applicant's claim language, as partially indicated here:

Claim	Partial ALU Calculation Language	Parallel Processing Language
Claim 1	performing at least partially the arithmetic operation	substantially in parallel
Claim 2	performing at least partially the multiplication	substantially in parallel
Claim 3	at least partially multiplying	substantially in parallel
Claim 6	performing at least a partial multiplication	substantially in parallel
Claim 13	at least partially multiplying	substantially in parallel
Claim 15	at least partially multiplying	substantially in parallel

Since the Examiner is required to consider *all words* in a claim when determining patentability, Applicant respectfully asserts that Otaguro's dependent, serial processes do not anticipate or render obvious Applicant's **partial ALU calculations** and **parallel processing**, as Applicant disclosed and claimed throughout the entirety of Applicant's application. Since i) serial and parallel processing are inapposite and the latter is not anticipated or rendered obvious by the former, and ii) Otaguro fails to disclose or suggest partial ALU calculations altogether, Applicant respectfully asserts that Otaguro cannot, and therefore does not, anticipate or render obvious Applicant's invention.

Accordingly, Applicant respectfully asserts that Otaguro fails to anticipate or render obvious Applicant's **partial ALU calculations** and **parallel processing**, as Applicant disclosed and claimed throughout the entirety of Applicant's application. Thus, Applicant respectfully asserts that all of Applicant's independent and dependent claims are novel and non-obvious. Earnestly believing Claims 1-2, 6-8, 13-15, and 17-19 recite patentable subject matter, Applicant respectfully requests reconsideration, and allowance, of the same.

6-7. The Examiner rejected Claims 3, 16, and 20 under 35 U.S.C. § 103(a) as being obvious over Otaguro in view of U.S. Pat. No. 6,321,248 to et al. ("Bonnet"). Respectfully, Applicant traverses and requests withdrawal.

As a preliminary matter, Applicant notes that since the Examiner limited the Examiner's analysis to Otaguro's FIG. 10 and Bonnet's FIG. 1, Applicant will likewise limit Applicant's response thereto.

As another preliminary matter, Applicant also renews at least all of the above arguments in reference to Otaguro. Applicant also respectfully notes that the Examiner may not have correctly understood or properly applied Bonnet.

First, regarding the rejection of Claim 3, the Examiner refers to the "first fixed-point format of the fast [sic] operand and the second fixed-point format of the second operand (output of 109" as VALSAT* and VALSAT. However, Bonnet's first and second operands are A and B, respectively, not VALSAT* or VALSAT. VALSAT* and VALSAT, on the other hand, are positive saturation values and negative saturation values, respectively. *See, e.g., Col. 10, lines 27-29.* Bonnet supplies one or the other to a multiplier 2 depending on whether or not an overflow is detected. *See id.* In other words, they are signals supplied to the multiplier 2 once the overflow status is already detected, and they are not otherwise used to determine the

overflow condition. As a result, the Examiner's observation that Bonnet's FIG. 1 "determin[es] a clamping value based on the first fixed-point format of the fast [sic] operand and the second fixed-point format of the second operand (VALSAT* and VALSAT into 2)" is incomplete, factually un-supported by Otaguro, or a non-sequitur.

Second, regarding the rejection of Claim 16, the Examiner references "receiving a clamp value to be output when clamping occurs" as 107. However, Otaguro's 107 is an Overflow Detector, not a "receiving a clamp value to be output when clamping occurs." In addition, the Examiner references a "clamp bit register input" from Otaguro's Col. 7, lines 24-25. However, Otaguro's Col. 7, lines 24-25 refers only to "detection result storage means for temporarily storing the contents of said detection means" and not in any way to a "clamp bit register input" as asserted by the Examiner. In addition, according to Bonnet:

> Regardless of the method used to determine if there is an overflow, the process according to the invention includes supplying the multiplexer with a positive saturation value VALSAT+ or a negative saturation value VALSAT-, if an overflow is detected.

Col. 10, lines 25-29. In other words, Bonnet's overflow is detected by either the i) NON-SAT, SAT, or SAT*, or ii) VALSAT* or VALSAT resulting from the Evaluation Unit 4.

Accordingly, both appear to be equivalent ways of presenting the overflow status to Bonnet's multiplexor 2. As a result, the Examiner's observation that Bonnet's FIG. 1 discloses "a multiplexor (2) comprising: an output wherein the multiplexor (input into 3) select[s] one of the clamp value register input (VALSAT) and the result register input (S) based upon a logical level of the clamp register (from 4) in order to make the selected input the output of the multiplexer" is incomplete, factually un-supported by Otaguro, or a non-sequitur.

Third, regarding the rejection of Claim 20, the Examiner references "a logical value of the final clamping predictor bit" as 107. However, Otaguro's 107 is an Overflow Detector, not a "a logical value of the final clamping predictor bit." In addition, the Examiner again refers to the "first fixed-point format of the fast [sic] operand and the second fixed-point format of the second operand" as VALSAT* and VALSAT. However, as previously explained, Bonnet's first and second operands are A and B, respectively, not VALSAT* or VALSAT. VALSAT* and VALSAT, on the other hand, are positive saturation values and negative saturation values, respectively. *See, e.g., Col. 10, lines 27-29.* Bonnet supplies one or the other to a multiplier 2 depending on whether or not an overflow is detected. *See id.* In other words, they are signals

supplied to the multiplier 2 once the overflow status is already detected, and they are not otherwise used to determine the overflow condition. As a result, the Examiner's observation that Bonnet's FIG. 1 "substitut[es] the operation result with the clamping value when it is determined that the operation result will exceed the representable value (by multiplexor in 2 in accumulator 3)" is incomplete, factually un-supported by Otaguro, or a non-sequitur.

As a result, it is currently impractical for Applicant to respond more fully to the Examiner's rejection of Claims 3, 16, and 20 under 35 U.S.C. § 103(a) as being obvious over Otaguro in view of Bonnet, although Applicant reserves the right to do so a future time if deemed necessary and the Examiner reasonably clarifies the Examiner's rejection.

In the meantime, Applicant respectfully asserts that all of Applicant's independent and dependent claims are novel and non-obvious. Earnestly believing Claims 3, 16, and 20 recite patentable subject matter, Applicant respectfully requests reconsideration, and allowance, of the same.

8. The Examiner objected to Claims 9-12 as being dependent upon a rejected base claim but indicated they would be allowable if re-written in independent form to include all of the limitations of the base claim and any intervening claims. As a result, Applicant amended Claims 10-12 to incorporate the limitations of Claim 8, as the Examiner suggested. Applicant also withdrew Claim 9 pending the Examiner's clarification of the objection to the drawings under 37 CFR 1.83(a).

9. The Examiner allowed Claims 4-5, for which Applicant is grateful.

10. The Examiner indicated that Applicant's arguments with respect to Claims 1-20 were considered, but are moot in view of the new ground(s) of rejection, which Applicant will interpret as the Examiner's removal of those rejections.

11. Applicant acknowledges that the Examiner made U.S. Pat. No. to 6,151,616 to Mahurin of record without relying thereupon.

CONCLUSION

Applicant believes Applicant has overcome the Examiner's rejection of 1-2, 6-8, 13-15, and 17-19 under 35 U.S.C. § 102(b) as being anticipated by Otaguro and Claims 3, 16, and 20 under 35 U.S.C. § 103(a) as being obvious over Otaguro in view of Bonnet. Applicant also believes Applicant has or will overcome the Examiner's objections to Claims 9-12. Moreover, Applicant believes Claims 1-20 are patentable. Thus, Applicant respectfully submits that all pending claims are in a condition for allowance, which Applicant respectfully requests. Applicant also seeks notification to that effect. Applicant also believes this Response should allow the Examiner to allow the above-referenced patent application to issue as a U.S. patent without further amendments to the specification or claims.

If questions arise, please telephone the undersigned attorney.